TS128MLR72V6L

168PIN PC133 Registered DIMM
1024MB With 64Mx4 CL3

Description

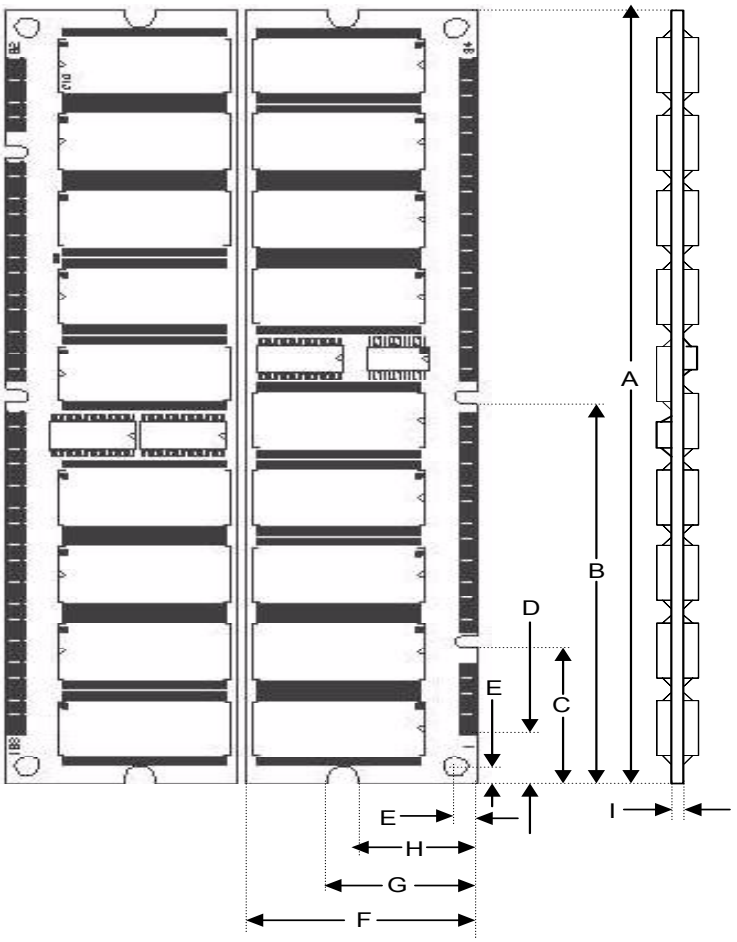
The TS128MLR72V6L is a 128M x 72 bits Synchronous Dynamic RAM high-density memory registered DIMM module. The TS128MLR72V6EL consists of 36pcs of CMOS 64Mx4bits Synchronous DRAMs in TSOP-II 400mil packages, 3pcs of drive ICs, 1pc of PLL and one 2048 bits serial EEPROM on a 168-pin printed circuit board. The TS128MLR72V6L is a Dual In-Line Memory Module and is intended for mounting into 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- Performance Range: PC-133.
- Burst Mode Operation.
- Auto and Self Refresh.
- Serial Presence Detect (SPD) with serial EEPROM
- LVTTL compatible inputs and outputs.
- Single 3.3V ± 0.3V power supply.
- MRS cycle with address key programs.
  Latency (Access from column address)
  Burst Length (1,2,4,8 & Full Page)
  Data Sequence (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.

Placement



PCB : 09-1350

Dimensions

Side	Millimeters	Inches
A	133.35±0.400	5.250±0.016
B	65.67	2.585
C	23.49	0.925
D	8.89	0.350
E	3.00	0.12
F	30.48±0.200	1.20±0.008
G	19.80	0.779
H	15.80	0.622
I	1.27±0.100	0.050±0.004

Pin Identification

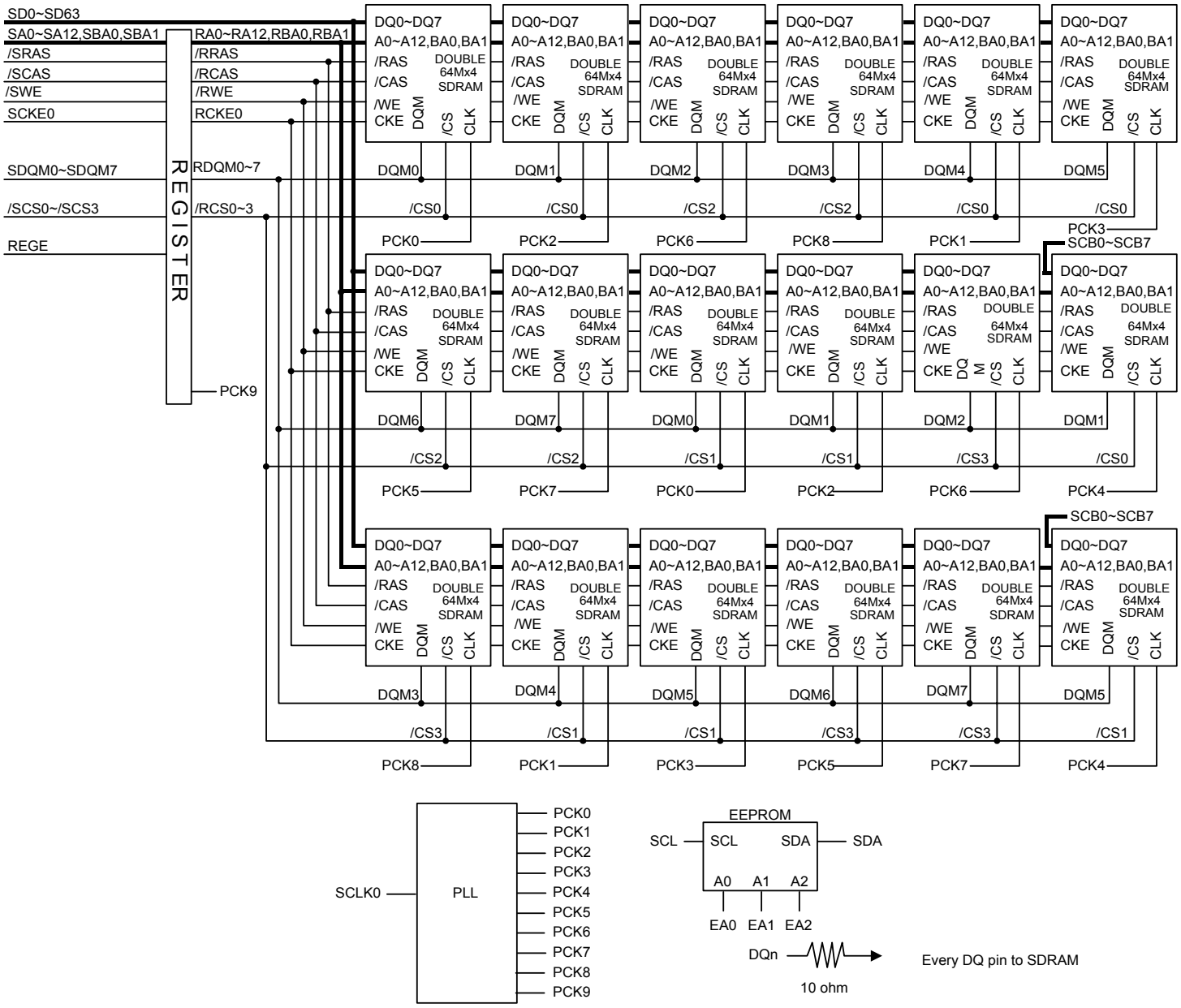
Symbol	Function
SA0~SA12	Address Input
SBA0, SBA1	Select Bank Address
SD0~SD63	Data Input / Output.
SCB0~SCB7	Check bit (data-in / data-out)
SCLK0	Clock Input.
SCKE0	Clock Enable Input.
/SCS0~/SCS3	Chip Select Input.
/SRAS	Row Address Strobe
/SCAS	Column Address Strobe
/SWE	Write Enable
SDQM0~SDQM7	Data (DQ) Mask
REGE	Register Enable
EA0~EA2	Address in EEPROM
SCL	Serial PD Clock
SDA	Serial PD Add/Data input/output
Vcc	+3.3 Voltage Power Supply
Vss	Ground
NC	No Connection

Pinouts:

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
01	Vss	43	Vss	85	Vss	127	Vss
02	SD0	44	NC	86	SD32	128	SCKE0
03	SD1	45	/SCS2	87	SD33	129	*/SCS3
04	SD2	46	SDQM2	88	SD34	130	SDQM6
05	SD3	47	SDQM3	89	SD35	131	SDQM7
06	Vcc	48	NC	90	Vcc	132	*SA13
07	SD4	49	Vcc	91	SD36	133	Vcc
08	SD5	50	NC	92	SD37	134	NC
09	SD6	51	NC	93	SD38	135	NC
10	SD7	52	SCB2	94	SD39	136	SCB6
11	SD8	53	SCB3	95	SD40	137	SCB7
12	Vss	54	Vss	96	Vss	138	Vss
13	SD9	55	SD16	97	SD41	139	SD48
14	SD10	56	SD17	98	SD42	140	SD49
15	SD11	57	SD18	99	SD43	141	SD50
16	SD12	58	SD19	100	SD44	142	SD51
17	SD13	59	Vcc	101	SD45	143	Vcc
18	Vcc	60	SD20	102	Vcc	144	SD52
19	SD14	61	NC	103	SD46	145	NC
20	SD15	62	NC	104	SD47	146	NC
21	SCB0	63	*SCKE1	105	SCB4	147	REGE
22	SCB1	64	Vss	106	SCB5	148	Vss
23	Vss	65	SD21	107	Vss	149	SD53
24	NC	66	SD22	108	NC	150	SD54
25	NC	67	SD23	109	NC	151	SD55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/SWE	69	SD24	111	/SCAS	153	SD56
28	SDQM0	70	SD25	112	SDQM4	154	SD57
29	SDQM1	71	SD26	113	SDQM5	155	SD58
30	/SCS0	72	SD27	114	*/SCS1	156	SD59
31	NC	73	Vcc	115	/SRAS	157	Vcc
32	Vss	74	SD28	116	Vss	158	SD60
33	SA0	75	SD29	117	SA1	159	SD61
34	SA2	76	SD30	118	SA3	160	SD62
35	SA4	77	SD31	119	SA5	161	SD63
36	SA6	78	Vss	120	SA7	162	Vss
37	SA8	79	NC	121	SA9	163	NC
38	SA10	80	NC	122	SBA0	164	NC
39	SBA1	81	NC	123	SA11	165	EA0
40	Vcc	82	SDA	124	Vcc	166	EA1
41	Vcc	83	SCL	125	NC	167	EA2
42	SCLK0	84	Vcc	126	*SA12	168	Vcc

*** Please refer Block Diagram**

Block Diagram



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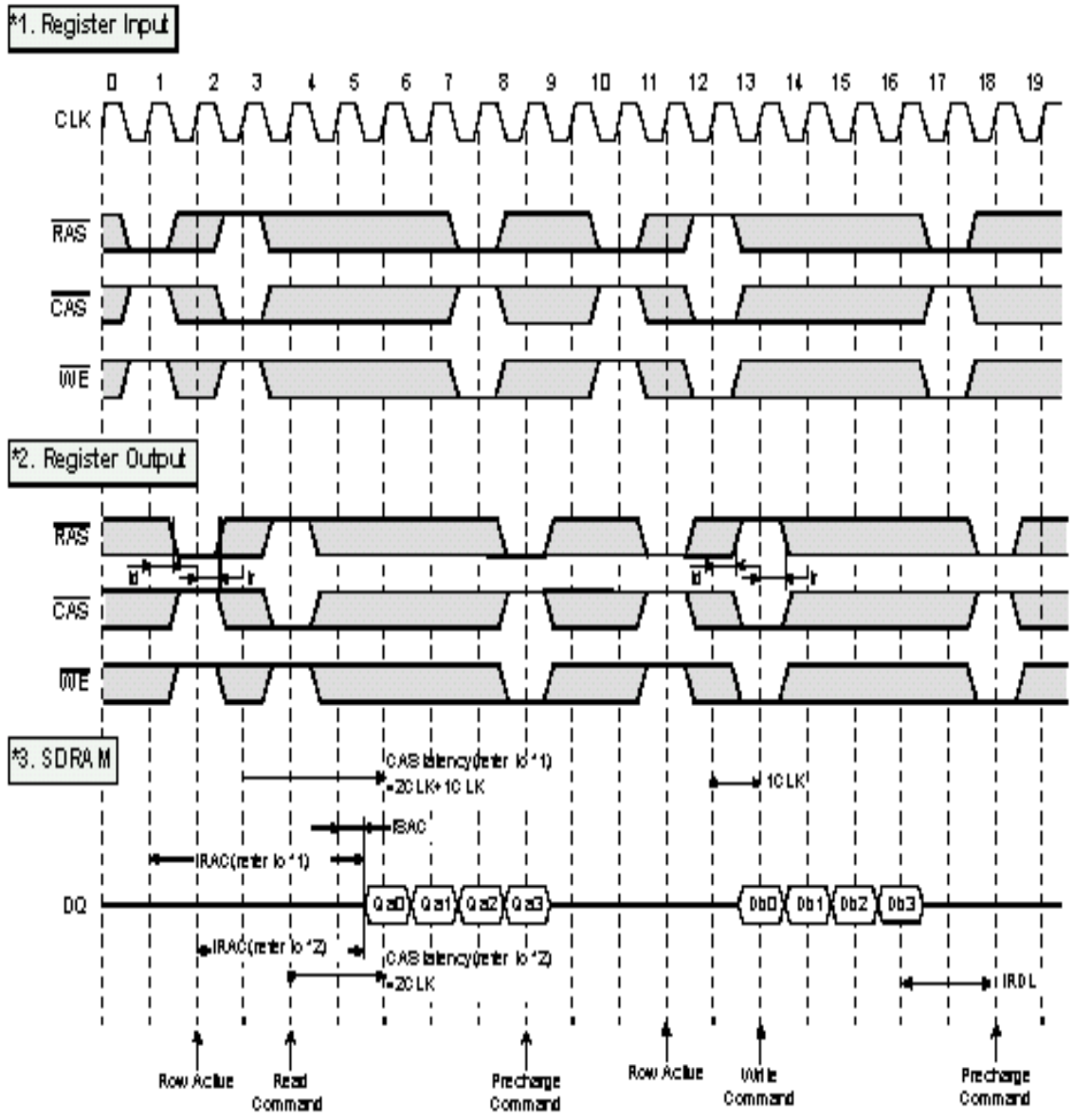
STANDARD TIMING DIAGRAM WITH PLL & REGISTER



td, tr = Delay of register (74ALVCF162835)

Notes : 1. In case of module timing, command cycles delayed 1CLK with respect to external input timing at the address and input signal because of the buffering in register (74ALVCF162835). Therefore, input/Output signals of read/write function should be issued 1CLK earlier as compared to Unbuffered DIMMs.

2. Dw is to be issued 1clock after write command in external timing because Dw is issued directly to module.

: Don't care

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0~4.6	V
Voltage on V_{DD} supply to Vss	V_{DD}, V_{DDQ}	-1.0~4.6	V
Storage temperature	T_{STG}	-55~+150	°C
Power dissipation	P_D	18	W
Short circuit current	I_{OS}	50	mA
Mean time between failure	MTBF	50	year
Temperature Humidity Burning	THB	85°C/85%, Static Stress	°C-%
Temperature Cycling Test	TC	0°C ~ 125°C Cycling	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Recommended operating conditions (Voltage referenced to Vss = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	IOH=-2mA
Output low voltage	V_{OL}	-	-	0.4	V	IOL=2mA
Input leakage current	I_{IL}	-10	-	10	uA	3

Note: 1. V_{IH} (max) = 5.6V AC .The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC .The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, TA = 23°C, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (SA_0~SA_{12}, SBA_0~ SBA_1)	C_{IN1}	-	15	pF
Input capacitance (/SRAS, /SCAS, /SWE)	C_{IN2}	-	15	pF
Input capacitance (SCKE0)	C_{IN3}	-	15	pF
Input capacitance (SCLK0)	C_{IN4}	-	20	pF
Input capacitance (/SCS0~/SCS3)	C_{IN5}	-	15	pF
Input capacitance (SDQM0~SDQM7)	C_{IN6}	-	15	pF
Data input/output capacitance (SD0~SD63)	C_{OUT}	-	22	pF
Data input/output capacitance (SCB0~SCB7)	C_{OUT}1	-	22	pF

DC CHARACTERISTICS

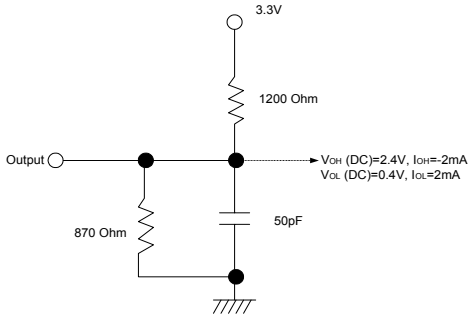
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	CAS Latency	Value	Unit	Note
Operating Current (One Bank Active)	I_{CC1}	Burst Length =1 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA		2,660	mA	1
Precharge Standby Current in power-down mode	I_{CC2}**P**	CKE≤V_{IL}(max), t_{CC}=10ns		422	mA	3
	I_{CC2}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞		74		
Precharge Standby Current in non power-down mode	I_{CC2}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns		1070	mA	3
	I_{CC2}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		362		
Active Standby Current in power-down mode	I_{CC3}**P**	CKE≤V_{IL}(max), t_{CC}=10ns		566	mA	3
	I_{CC3}**PS**	CKE & CLK≤V_{IL}(max), t_{CC}=∞		218		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3}**N**	CKE≥V_{IH}(min), /CS≥V_{IH}(min), t_{CC}=10ns Input signals are changed one time during 20ns		1,430	mA	3
	I_{CC3}**NS**	CKE≥V_{IH}(min), CLK≤V_{IL}(max), t_{CC}=∞ Input signals are stable		902		
Operating Current (Bust Mode)	I_{CC4}	I_{OL}= 0 mA Page Burst t_{CCD} = 2CLKs		3,020	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		4,640	mA	2
Self Refresh Current	I_{CC6}	CKE≤0.2V		458	mA	3

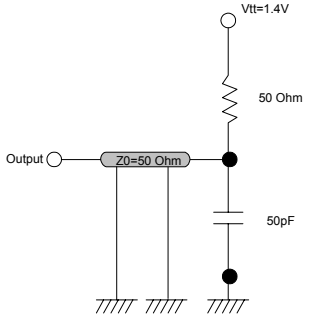
Note: 1. Measured with outputs open.
2. Refresh period is 64ms.
3. Measured with 1 PLL & 3 Drive ICs
4. Unless otherwise noticed, input swing level is CMOS (V_{IH}/\V_{IL}=V_{DDQ}/V_{SSQ})

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V±0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
AC Input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER (AC operating conditions unless otherwise noted)

Parameter	Symbol	Value	Unit	Note
/RAS to /CAS delay	t_{RCD}(min)	15	ns	1
Row precharge time	t_{RP}(min)	20	ns	1
Row active time	t_{RAS}(min)	45	ns	1
	t_{RAS}(max)	100	us	
Row cycle time	t_{RC}(min)	65	ns	1
Last data in to new col. address delay	t_{CDL}(min)	1	CLK	2
Last data in to row precharge	t_{RDL}(min)	2	CLK	2
Last data in to Active delay	t_{DAL}	2CLK+20ns		
Last data in to burst stop	t_{BDL}(min)	1	CLK	2
Col. address to col. address delay	t_{CCD}(min)	1	CLK	3
Number of valid output data	CAS latency=3	2	ea	4

Note:
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Refer to the individual component, not the whole module.

Parameter		Symbol	Value		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	t_{CC}	7.5	1000	ns	1
CLK to valid output delay	CAS latency=3	t_{SAC}		5.4	ns	1, 2
Output data hold time	CAS latency=3	t_{OH}	3		ns	1, 2
CLK high pulse width		t_{CH}	2.5		ns	3
CLK low pulse width		t_{CL}	2.5		ns	3
Input setup time		t_{SS}	1.5		ns	3
Input hold time		t_{SH}	0.8		ns	3
CLK to output in Low-Z		t_{SLZ}	1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}		5.4	ns	1

Note: 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)= 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			SCKEn-1	SCKEn	/SCS	/SRAS	/SCAS	/SWE	SDQM	$SBA_{0,1}$	SA_{10}/AP	SA_{12},SA_{11},SA_0~SA_9	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
				L									3
	Self Refresh	Entry			L	H	H	H	X	X			3
		Exit	L	H	H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (SA_0~SA_9, SA_{11})	4
	Auto Precharge Enable										H		4, 5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (SA_0~SA_9, SA_{11})	4
	Auto Precharge Enable										H		4, 5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
SDQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

Note:

1. OP Code : Operand Code
   SA_0~SA_{12}, SBA_0~SBA_1 : Program keys. (@MRS)
2. MRS can be issued only at both banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatically precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at both banks precharge state.
4. SBA_0~SBA_1: Bank select address.
   If both SBA_0 and SBA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both SBA_0 is "Low" and SBA_1 is "High" at read, write, row active and precharge, bank B is selected.
   If both SBA_0 is "High" and SBA_1 is "Low" at read, write, row active and precharge, bank C is selected.
   If both SBA_0 and SBA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If SA_{10}/AP is "High" at row precharge, SBA_0 and SBA_1 is ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. SDQM sampled at positive going edged of a CLK masks the data-in at the very CLK (Write SDQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read SDQM latency is 2)

Serial Presence Detect Specification

Serial Presence Detect			
Byte No.	Function Described	Standard Specification	Vendor Part
0	# of Bytes Written into Serial Memory	128bytes	80
1	Total # of Bytes of S.P.D Memory	256bytes	08
2	Fundamental Memory Type	SDRAM	04
3	# of Row Addresses on this Assembly	13	0D
4	# of Column Addresses on this Assembly	11	0B
5	# of Module Banks on this Assembly	2 bank	02
6	Data Width of this Assembly	72bits	48
7	Data Width Continuation	0	00
8	Voltage Interface Standard of this Assembly	LVTTL3.3V	01
9	SDRAM Cycle Time (highest CAS latency)	7.5ns	75
10	SDRAM Access from Clock (highest CL)	5.4ns	54
11	DIMM configuration type (non-parity, ECC)	ECC	02
12	Refresh Rate Type	7.8us/Self Refresh	82
13	Primary SDRAM Width	X4	04
14	Error Checking SDRAM Width	X4	04
15	Min Clock Delay Back to Back Random Address	1 clock	01
16	Burst Lengths Supported	1,2,4,8 & Full page	8F
17	Number of banks on each SDRAM device	4 bank	04
18	CAS # Latency	3	04
19	CS # Latency	0 clock	01
20	Write Latency	0 clock	01
21	SDRAM Module Attributes	Registered DQM, address/control inputs and on-card PLL	16
22	SDRAM Device Attributes: General	Prec All, Auto Prec, R/W Burst	0E
23	SDRAM Cycle Time (2^{nd} highest CL)	10ns	A0
24	SDRAM Access from Clock (2^{nd} highest CL)	6ns	60
25	SDRAM Cycle Time (3^{rd} highest CL)	0ns	00
26	SDRAM Access from Clock (3^{rd} highest CL)	0ns	00
27	Minimum Row Precharge Time	20ns	14
28	Minimum Row Active to Row Activate	15ns	0F
29	Minimum RAS to CAS Delay	20ns	14
30	Minimum RAS Pulse Width	45ns	2D
31	Density of Each Bank on Module	512MB	80
32	Command/Address Setup Time	1.5ns	15

33	Command/Address Hold Time	0.8ns	08
34	Data Signal Setup Time	1.5ns	15
35	Data Signal Hold Time	0.8ns	08
36-61	Superset Information	-	00
62	SPD Data Revision Code	JEDEC 2	02
63	Checksum for Bytes 0-62	-	22
64-71	Manufacturers JEDEC ID code per JEP-108E	Transcend	7F, 4F
72	Manufacturing Location	T	54
73-90	Manufacturers Part Number	TS128MLR72V6L	54 53 31 32 38 4D 4C 52 37 32 56 36 4C 20 20 20 20 20
91-92	Revision Code	-	0
93-94	Manufacturing Date	By Manufacturer	Variable
95-98	Assembly Serial Number	By Manufacturer	Variable
99-125	Manufacturer Specific Data	-	0
126	Intel Specification Frequency	-	64
127	Intel Specification CAS# Latency/Clock Signal Support	CL=3 Clock 0	84
128~	Unused Storage Locations	Open	FF